SBOS333B − JULY 2005 − REVISED OCTOBER 2005

Precision, Gain of 0.2 Level Translation DIFFERENCE AMPLIFIER

FEATURES

- GAIN OF 0.2 TO INTERFACE ±10V SIGNALS TO SINGLE-SUPPLY ADCs
- GAIN ACCURACY: ±0.024% (max)
- WIDE BANDWIDTH: 1.5MHz
- HIGH SLEW RATE: 15V/µs
- LOW OFFSET VOLTAGE: ±100µV
- LOW OFFSET DRIFT: ±1.5µV/°C
- SINGLE-SUPPLY OPERATION DOWN TO 1.8V

APPLICATIONS

- INDUSTRIAL PROCESS CONTROLS
- INSTRUMENTATION
- DIFFERENTIAL TO SINGLE-ENDED CONVERSION
- AUDIO LINE RECEIVERS

DESCRIPTION

The INA159 is a high slew rate, G = 1/5 difference amplifier consisting of a precision op amp with a precision resistor network. The gain of 1/5 makes the INA159 useful to couple ±10V signals to single-supply analog-to-digital converters (ADCs), particularly those operating on a single +5V supply. The on-chip resistors are laser-trimmed for accurate gain and high common-mode rejection. Excellent temperature coefficient of resistance (TCR) tracking of the resistors maintains gain accuracy and common-mode rejection over temperature. The input common-mode voltage range extends beyond the positive and negative supply rails. It operates on a total of +1.8V to +5.5V single or split supplies. The INA159 reference input uses two resistors for easy mid-supply or reference biasing.

The difference amplifier is the foundation of many commonly-used circuits. The INA159 provides this circuit function without using an expensive external precision resistor network. The INA159 is available in an MSOP-8 surface-mount package and is specified for operation over the extended industrial temperature range, −40°C to +125°C.

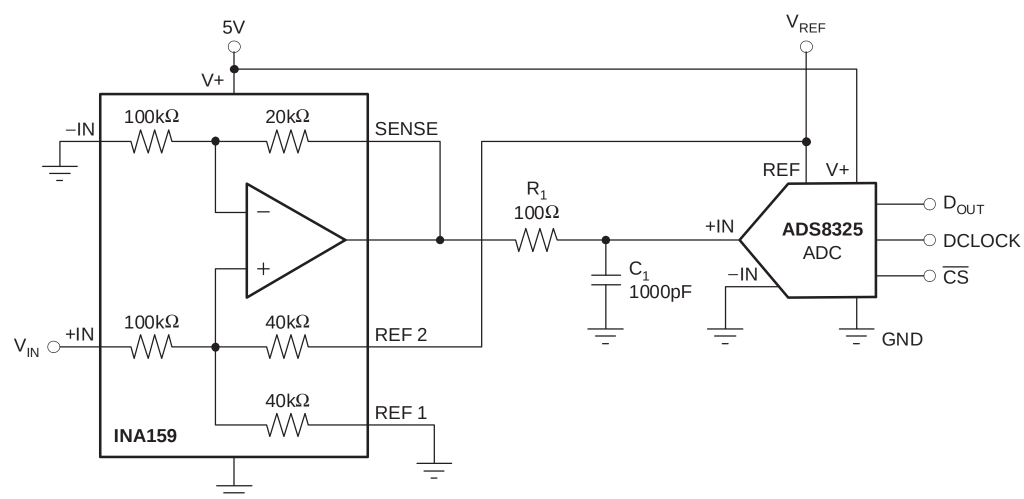


Figure 1. Typical Application

ABSOLUTE MAXIMUM RATINGS(1)

Supply Voltage	+5.5V
Signal Input Terminals (−IN and +IN), Voltage	±30V
Reference (REF 1 and REF2) and Sense Pins	
Current	±10mA
Voltage	(V−) − 0.5V to (V+) + 0.5V
Output Short Circuit	Continuous
Operating Temperature	−40°C to +150°C
Storage Temperature	−65°C to +150°C
Junction Temperature	+150°C
ESD Rating	
Human Body Model	4000V
Charged Device Model	1000V

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not supported.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

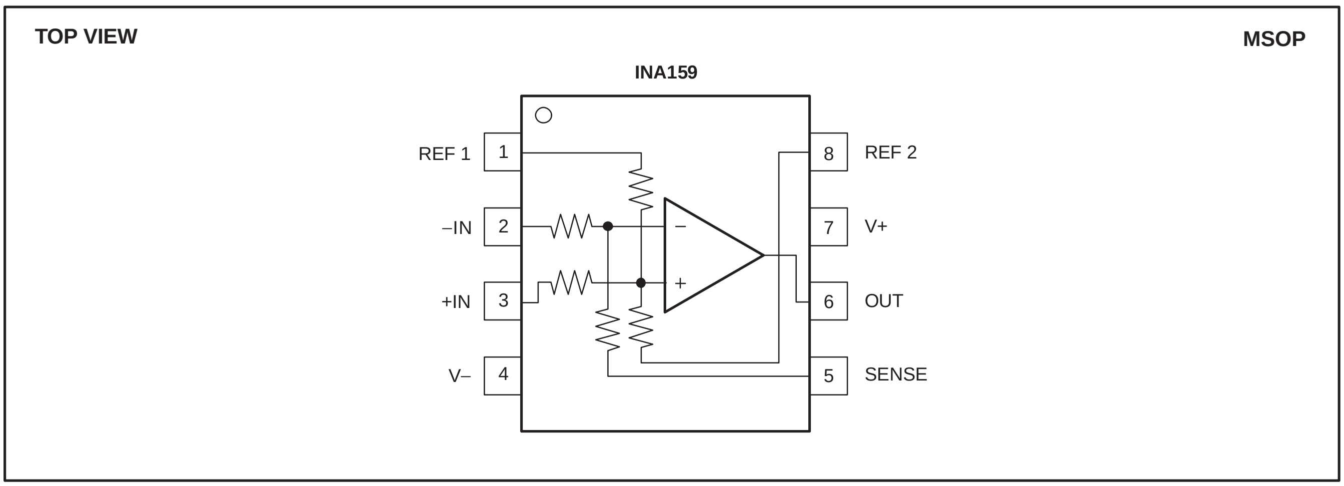
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	PACKAGE MARKING
INA159	MSOP-8	DGK	CJB

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

PIN CONFIGURATIONS



ELECTRICAL CHARACTERISTICS: V_S = +5V

Boldface limits apply over the specified temperature range, **T_A = −40°C to +125°C.**

At T_A = +25°C, R_L = 10kΩ connected to V_S/2, REF pin 1 connected to ground, and REF pin 2 connected to V_{REF} = 5V, unless otherwise noted.

PARAMETER		CONDITIONS	INA159 MIN	TYP	MAX	UNIT
OFFSET VOLTAGE(1)		RTO				
Initial (1)	V_{OS}	V_S = ±2.5V, Reference and Input Pins Grounded		±100	±500	µV
vs Temperature				**±1.5**		**µV/°C**
vs Power Supply	PSRR	V_S = ±0.9V to ±2.75V		±20	±100	µV/V
Reference Divider Accuracy(2)				±0.002	±0.024	%
over Temperature				**±0.002**		**%**
INPUT IMPEDANCE(3)						
Differential				240		kΩ
Common-Mode				60		kΩ
INPUT VOLTAGE RANGE		RTI				
Common-Mode Voltage Range	V_{CM}					
Positive				17.5		V
Negative				−12.5		V
Common-Mode Rejection Ratio	CMRR	V_{CM} = −10V to +10V, R_S = 0Ω	80	96		dB
over Temperature				**94**		**dB**
OUTPUT VOLTAGE NOISE(4)		RTO				
f = 0.1Hz to 10Hz				10		μV_{PP}
f = 10kHz				30		nV/√Hz
GAIN		V_{REF2} = 4.096V, R_L Connected to GND, (V_{IN+}) − (V_{IN-}) = −10V to +10V, V_{CM} = 0V				
Initial	G			0.2		V/V
Error				±0.005	±0.024	%
vs Temperature				**±1**		**ppm/°C**
Nonlinearity				±0.0002		% of FS
OUTPUT						
Voltage, Positive		V_{REF2} = 4.096V, R_L Connected to GND	(V+) − 0.1	(V+) − 0.02		V
Voltage, Negative		V_{REF2} = 4.096V, R_L Connected to GND	(V−) + 0.048	(V−) + 0.01		V
Current Limit, Continuous to Common				±60		mA
Capacitive Load				See Typical Characteristic		pF
Open-Loop Output Impedance	R_O	f = 1MHz, I_O = 0		110		Ω
FREQUENCY RESPONSE						
Small-Signal Bandwidth		−3dB		1.5		MHz
Slew Rate	SR			15		V/µs
Settling Time, 0.01%	t_S	4V Output Step, C_L = 100pF		1		µs
Overload Recovery Time		50% Overdrive		250		ns
POWER SUPPLY						
Specified Voltage Range	V_S			+5		V
Operating Voltage Range			+1.8		+5.5	V
Quiescent Current	I_Q	I_O = 0mA, V_S = ±2.5V, Reference and Input Pins Grounded		1.1	1.5	mA
TEMPERATURE RANGE						
Specified Range			−40		+125	°C
Operating Range			−40		+150	°C
Storage Range			−65		+150	°C
Thermal Resistance	θ_{JA}					
MSOP-8		Surface-Mount		150		°C/W

(1) Includes effects of amplifier input bias and offset currents.
(2) Reference divider accuracy specifies the match between the reference divider resistors using the configuration in Figure 2.
(3) Internal resistors are ratio matched but have ±20% absolute value.
(4) Includes effects of amplifier input current noise and thermal noise contribution of resistor network.

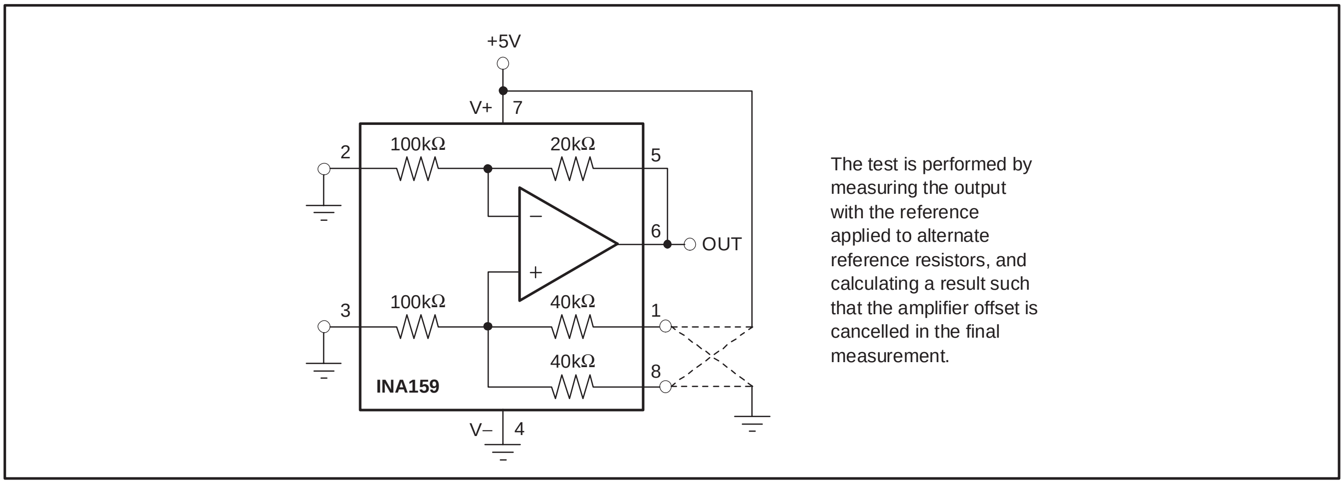
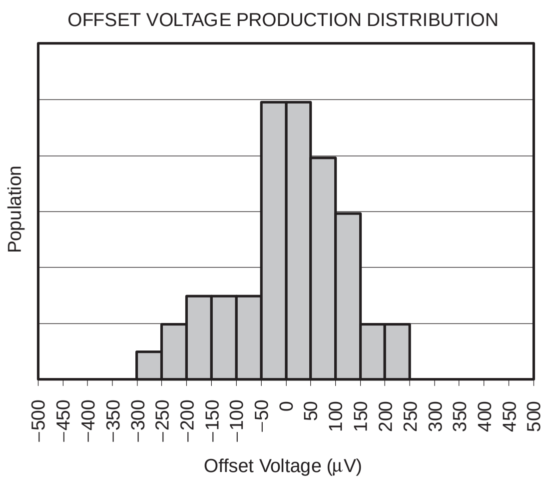
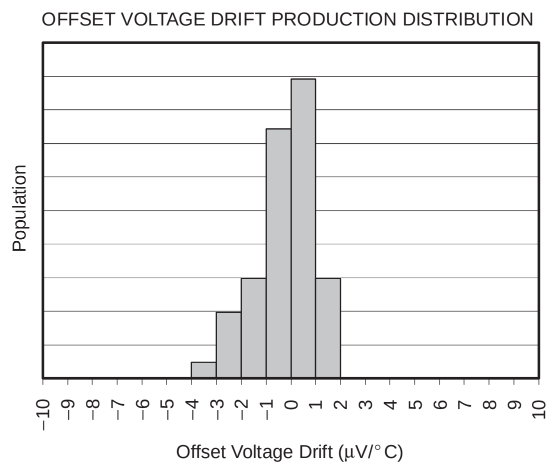


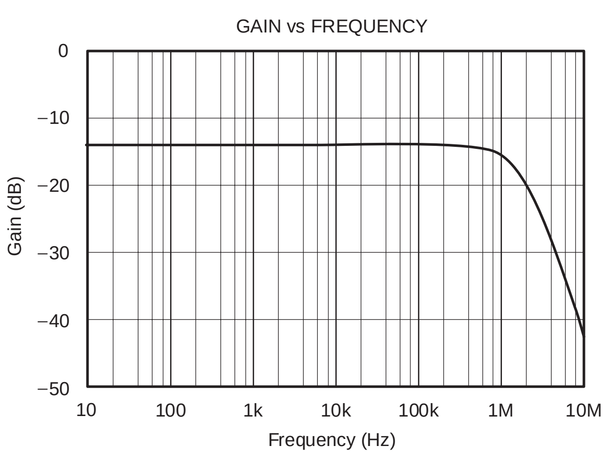
Figure 2. Test Circuit for Reference Divider Accuracy

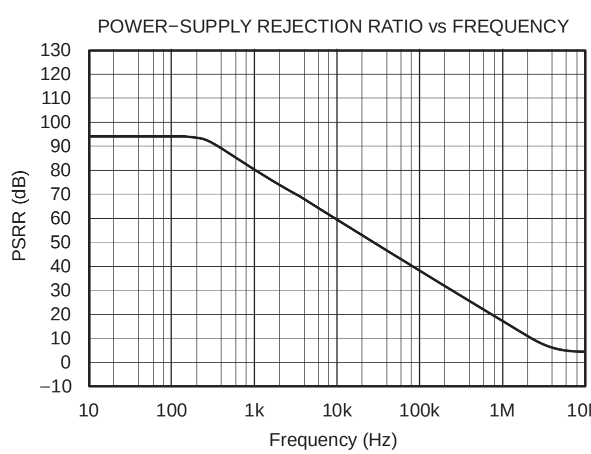
TYPICAL CHARACTERISTICS

At T_A = +25°C, R_L = 10kΩ connected to V_S/2, REF pin 1 connected to ground, and REF pin 2 connected to V_{REF} = 5V, unless otherwise noted.



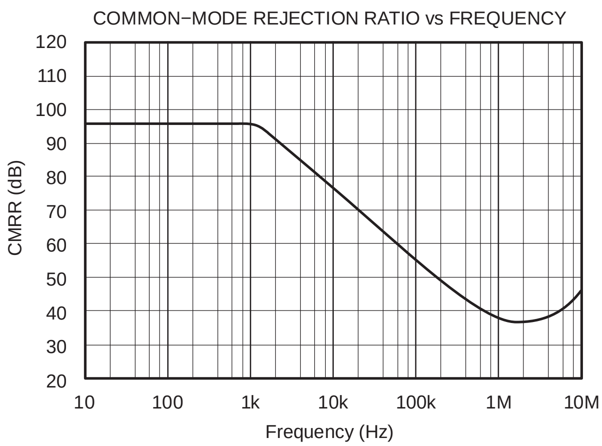


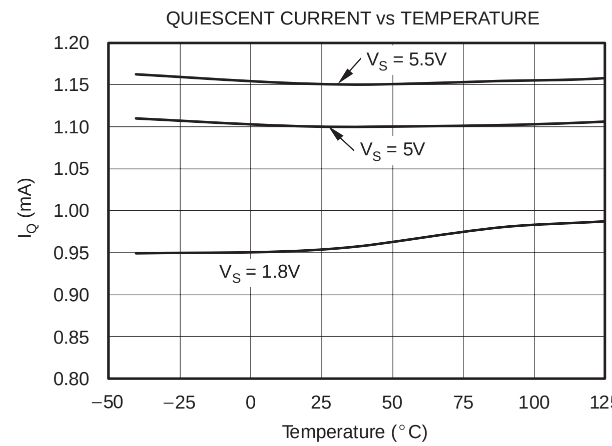


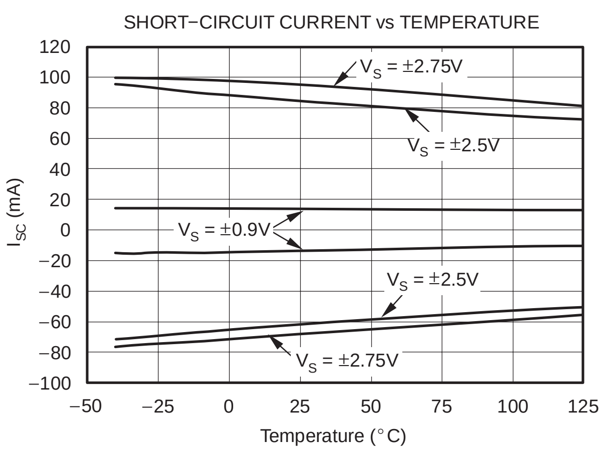


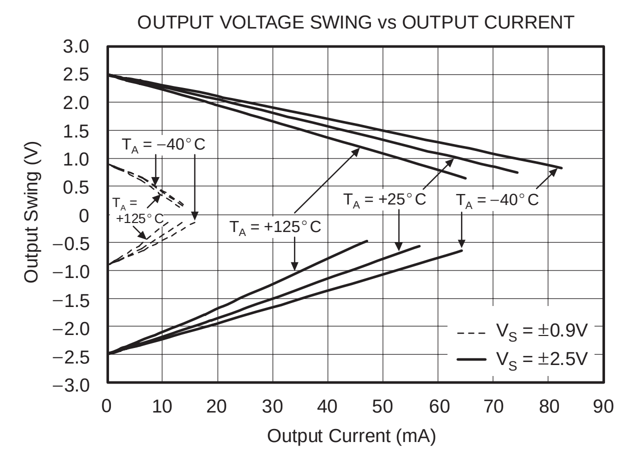
TYPICAL CHARACTERISTICS (continued)

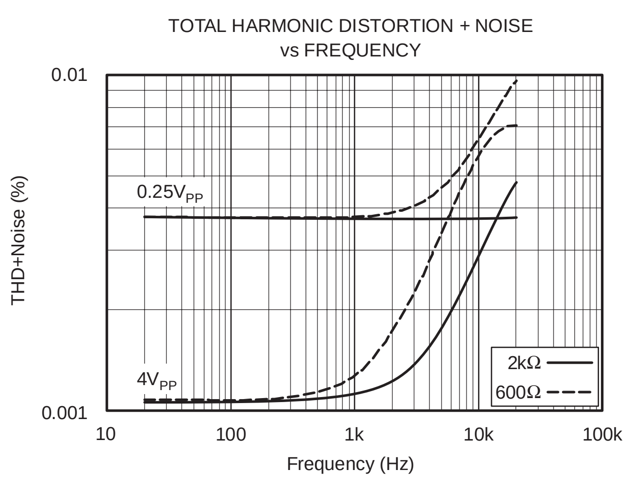
At T_A = +25°C, R_L = 10kΩ connected to V_S/2, REF pin 1 connected to ground, and REF pin 2 connected to V_{REF} = 5V, unless otherwise noted.

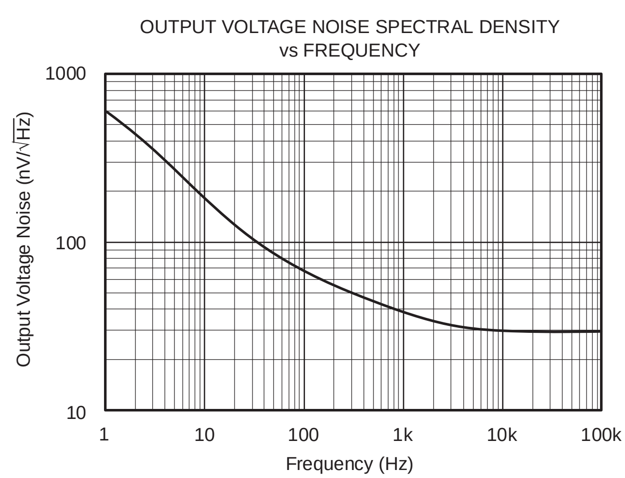








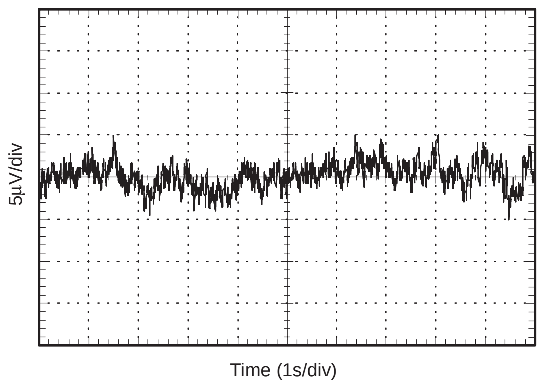




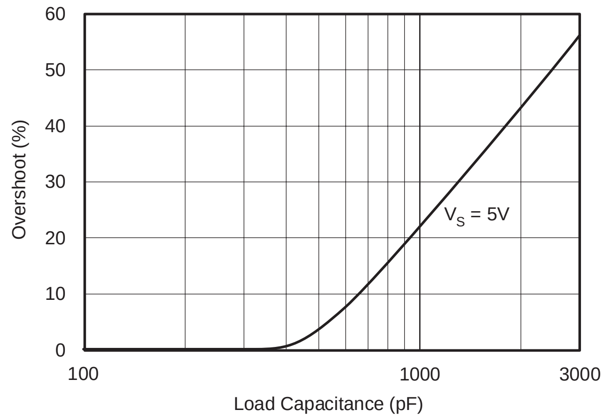
TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, R_L = 10kΩ connected to V_S/2, REF pin 1 connected to ground, and REF pin 2 connected to V_{REF} = 5V, unless otherwise noted.

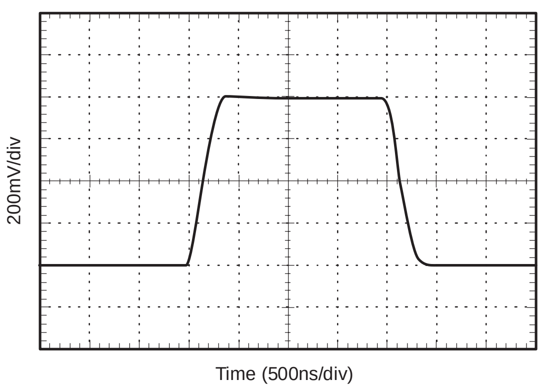
0.1Hz TO 10Hz NOISE



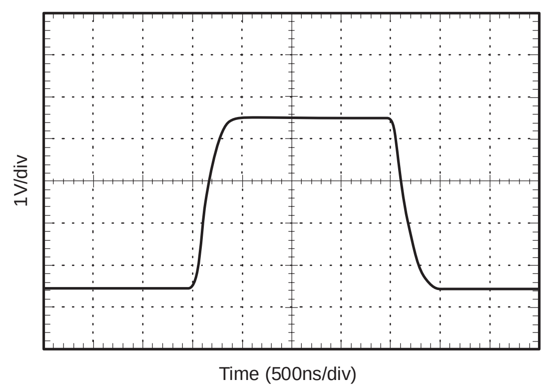
SMALL−SIGNAL OVERSHOOT vs LOAD CAPACITANCE



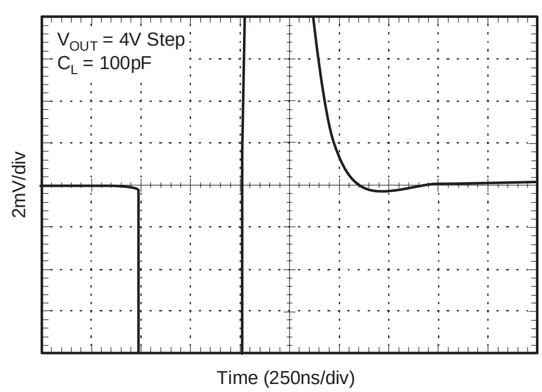
SMALL−SIGNAL STEP RESPONSE



LARGE−SIGNAL STEP RESPONSE



SETTLING TIME



APPLICATION INFORMATION

The internal op amp of the INA159 has a rail-to-rail common-mode voltage capability at its inputs. A rail-to-rail op amp allows the use of ±10V inputs into a circuit biased to 1/2 of a 5V reference (2.5V quiescent output). The inputs to the op amp will swing from approximately 400mV to 3.75V in this application.

The unique input topology of the INA159 eliminates the input offset transition region typical of most rail-to-rail complementary stage operational amplifiers. This allows the INA159 to provide superior glitch- and transition-free performance over the entire common-mode range.

Good layout practice includes the use of a 0.1µF bypass capacitor placed closely across the supply pins.

COMMON-MODE RANGE

The common-mode range of the INA159 is a function of supply voltage and reference. Where both pins, REF1 and REF2, are connected together:

$$V_{CM+} = (V+) + 5[(V+) - V_{REF}] \quad (1)$$

$$V_{CM-} = (V-) - 5[V_{REF} - (V-)] \quad (2)$$

Where one REF pin is connected to the reference, and the other pin grounded (1/2 reference connection):

$$V_{CM+} = (V+) + 5[(V+) - (0.5V_{REF})] \quad (3)$$

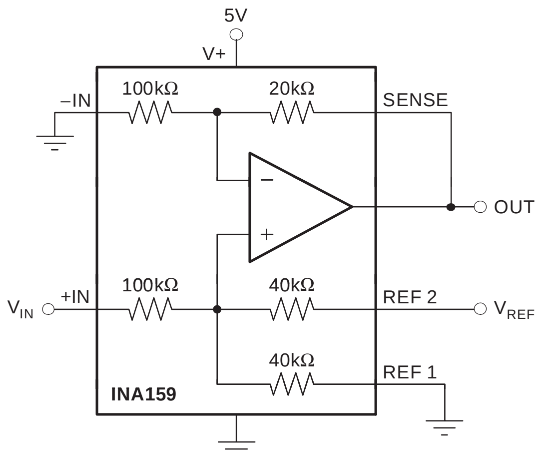
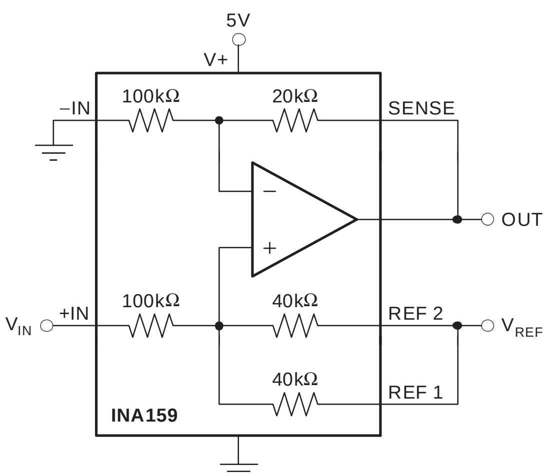
$$V_{CM-} = (V-) - 5[(0.5V_{REF}) - (V-)] \quad (4)$$

Some typical values are shown in Table 1.

Table 1. Common-Mode Range For Various Supply and Reference Voltages

REF 1 and REF 2 Connected Together				
V+	V−	V_{REF}	V_{CM+}	V_{CM-}
5	0	3	15	−15
5	0	2.5	17.5	−12.5
5	0	1.25	23.75	−6.25
1/2 Reference Connection				
V+	V−	V_{REF}	V_{CM+}	V_{CM-}
5	0	5	17.5	−12.5
5	0	4.096	19.76	−10.24
5	0	2.5	23.75	−6.25
3.3	0	3.3	11.55	−8.25
3.3	0	2.5	13.55	−6.25
3.3	0	1.25	16.675	−3.125

Table 2. Input and Output Relationships for Various Reference and Connection Combinations

<table>
<tr><th>V_{REF} (V)</th><th>REF CONNECTION</th><th>V_{OUT} for V_{IN} = 0 (V)</th><th>LINEAR V_{IN} RANGE (V)</th><th>USEFUL V_{OUT} SWING (V)</th></tr>
<tr><td>5</td><td rowspan="5">
</td><td>2.5</td><td>+10
0
−10</td><td>4.5
(±2V swing)
0.5</td></tr>
<tr><td>4.096</td><td>2.048</td><td>+10
0
−10</td><td>4.048
(±2V swing)
0.048</td></tr>
<tr><td>3.3</td><td>1.65</td><td>+10
0
−7.885</td><td>3.65
(−1.577V, +2V swing)
0.048</td></tr>
<tr><td>2.5</td><td>1.25</td><td>+10 (also +5)
0
−6 (also −5)</td><td>3.25
(−1.2V, +2V swing)
0.048</td></tr>
<tr><td>1.8</td><td>0.9</td><td>+10
0
−4.26</td><td>2.9
(−0.852V, +2V swing)
0.048</td></tr>
<tr><td>2.5</td><td rowspan="3">
</td><td>2.5</td><td>+10
0
−10</td><td>4.5
(±2V swing)
0.5</td></tr>
<tr><td>1.8</td><td>1.8</td><td>+10
0
−8.76</td><td>3.8
(−1.752V, +2V swing)
0.048</td></tr>
<tr><td>1.2</td><td>1.2</td><td>+10
0
−5.76</td><td>3.2
(−1.15V, +2V swing)
0.048</td></tr>
</table>

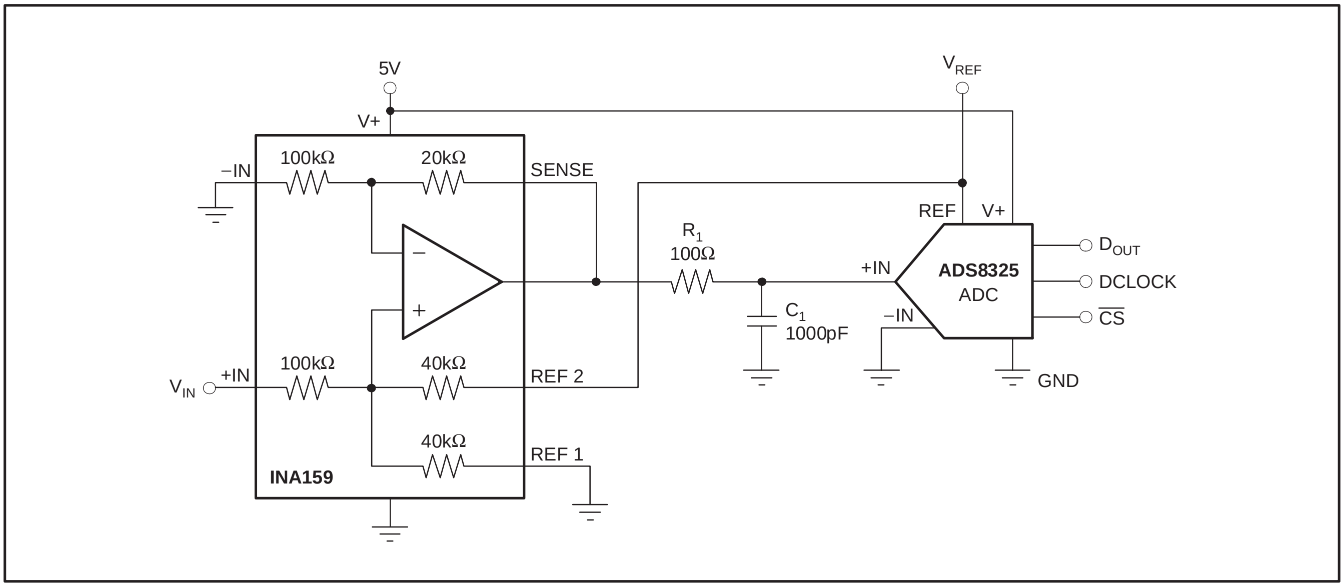


Figure 3. Typical Application Circuit Interfacing to Medium-Speed, Single-Supply ADCs

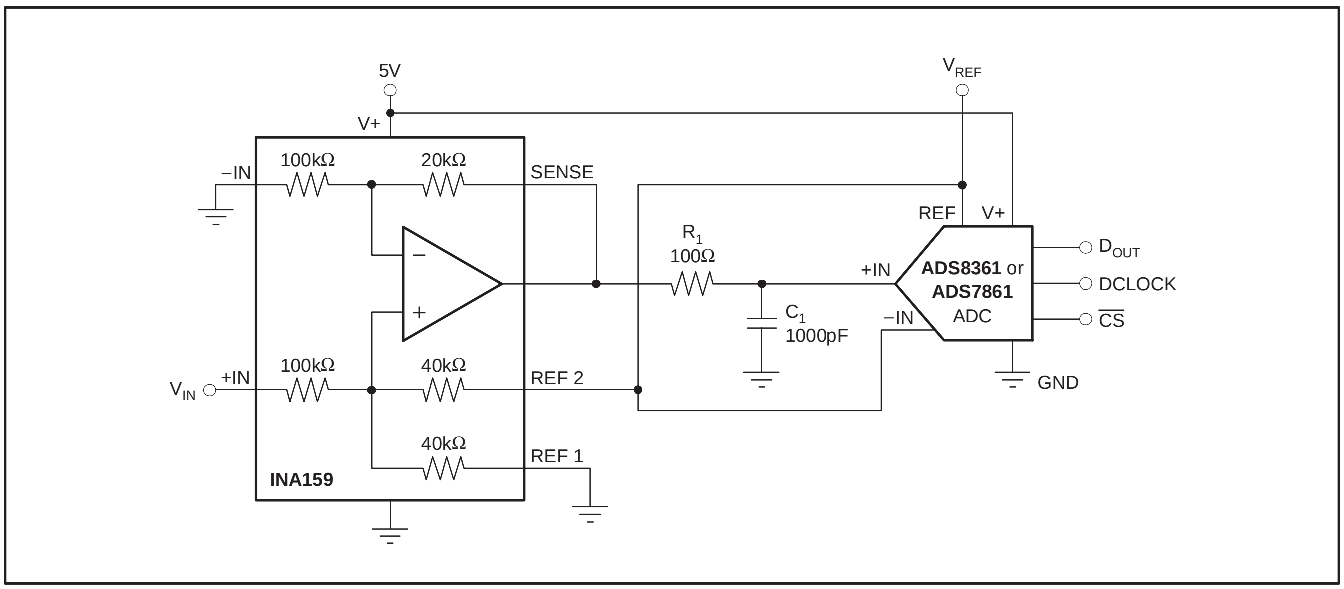
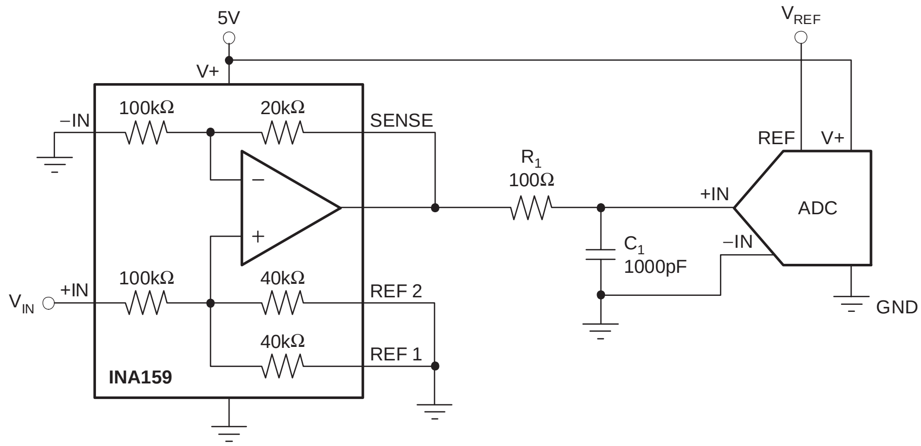
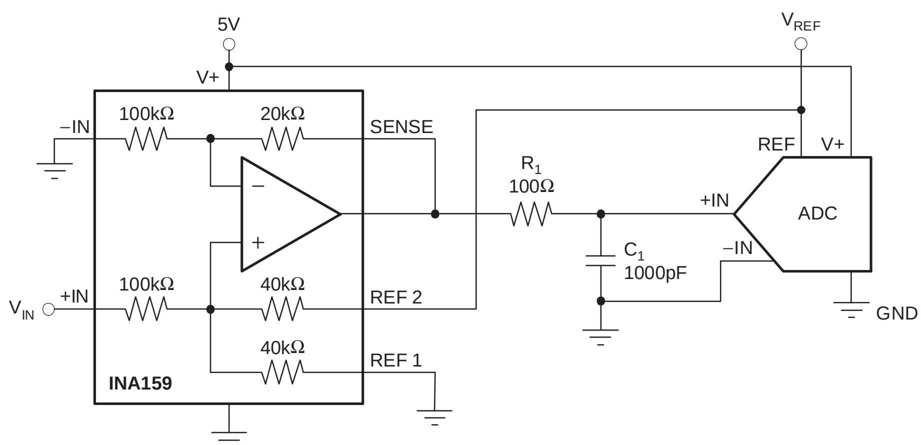


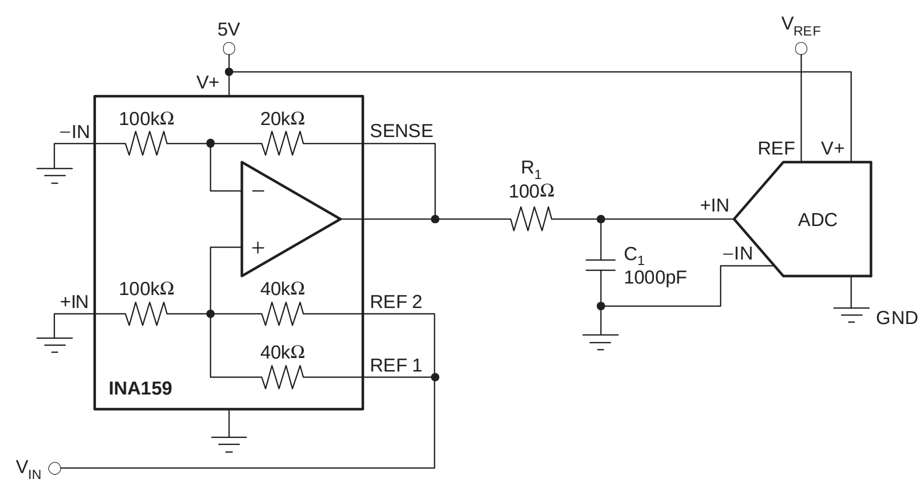
Figure 4. Typical Application Circuit Interfacing to Medium-Speed, Single-Supply ADCs with Pseudo-Differential Inputs (such as the ADS7861 and ADS8361)



a) Unipolar, Noninverting, G = 0.2



b) Bipolar, Noninverting, G = 0.2



c) Unipolar, Unity Gain

Figure 5. Basic INA159 Configurations

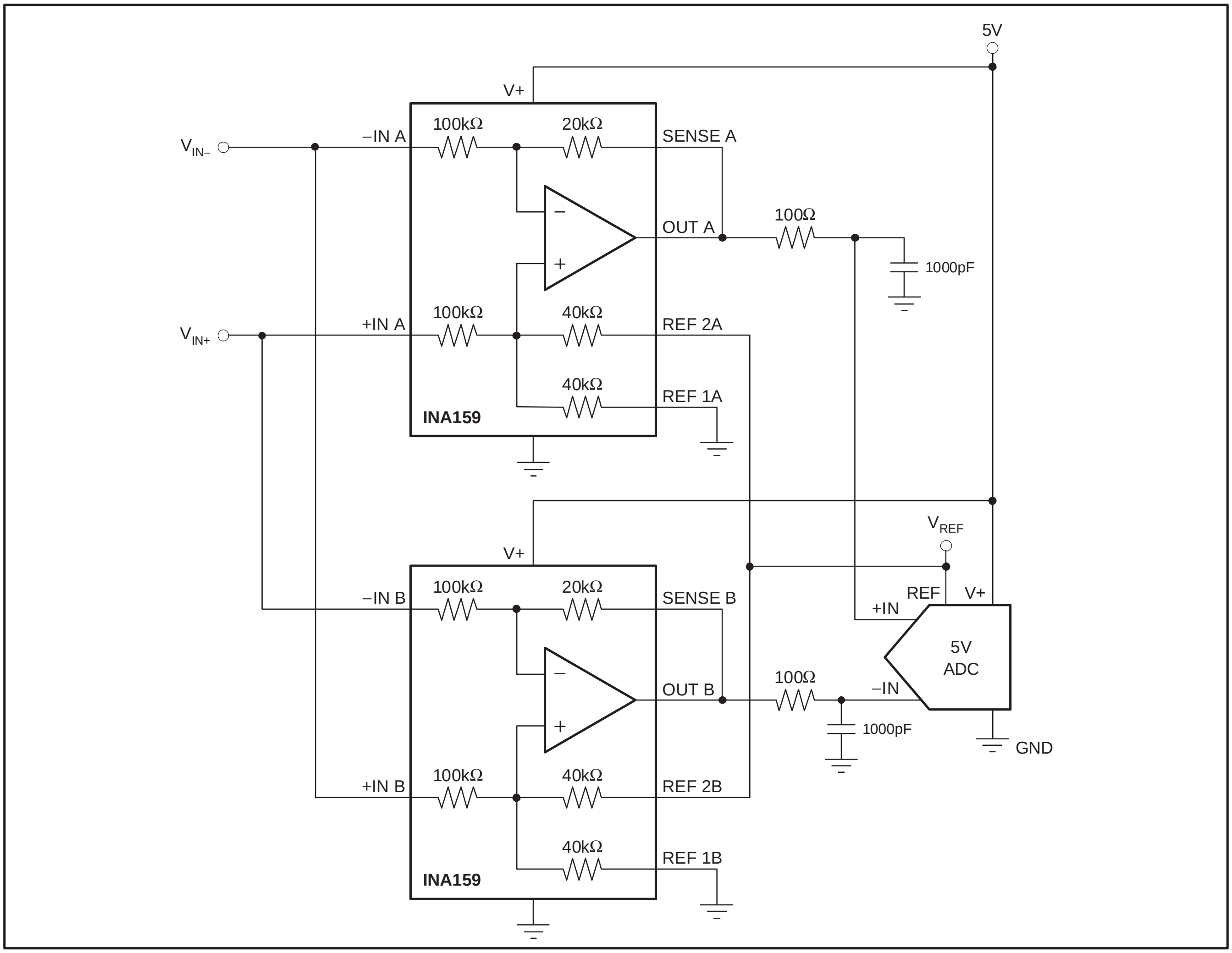


Figure 6. Differential ADC Drive

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
INA159AIDGKR	ACTIVE	MSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
INA159AIDGKRG4	ACTIVE	MSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
INA159AIDGKT	ACTIVE	MSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
INA159AIDGKTG4	ACTIVE	MSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

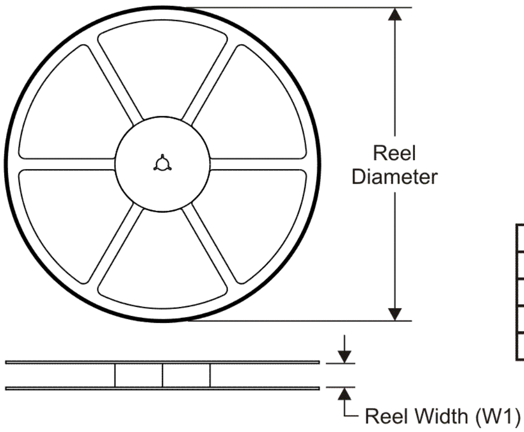
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

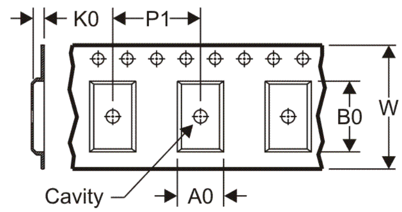
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

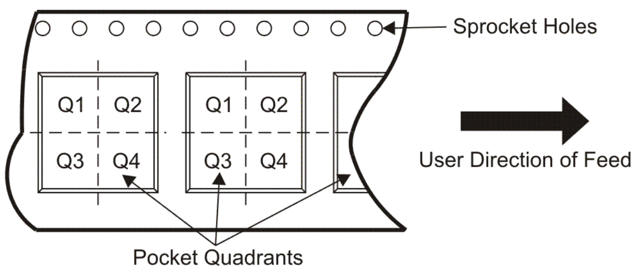


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

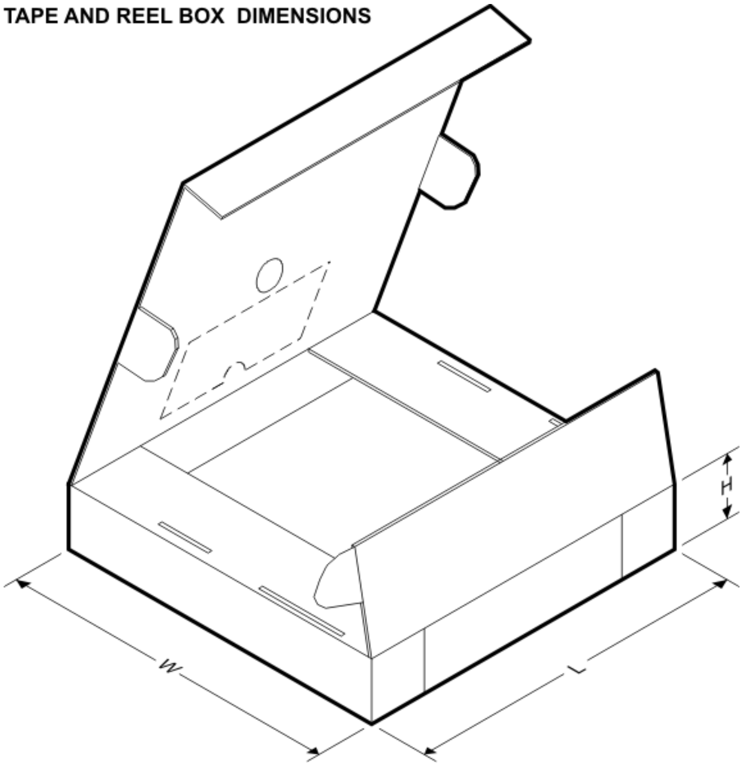
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
INA159AIDGKR	MSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
INA159AIDGKT	MSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

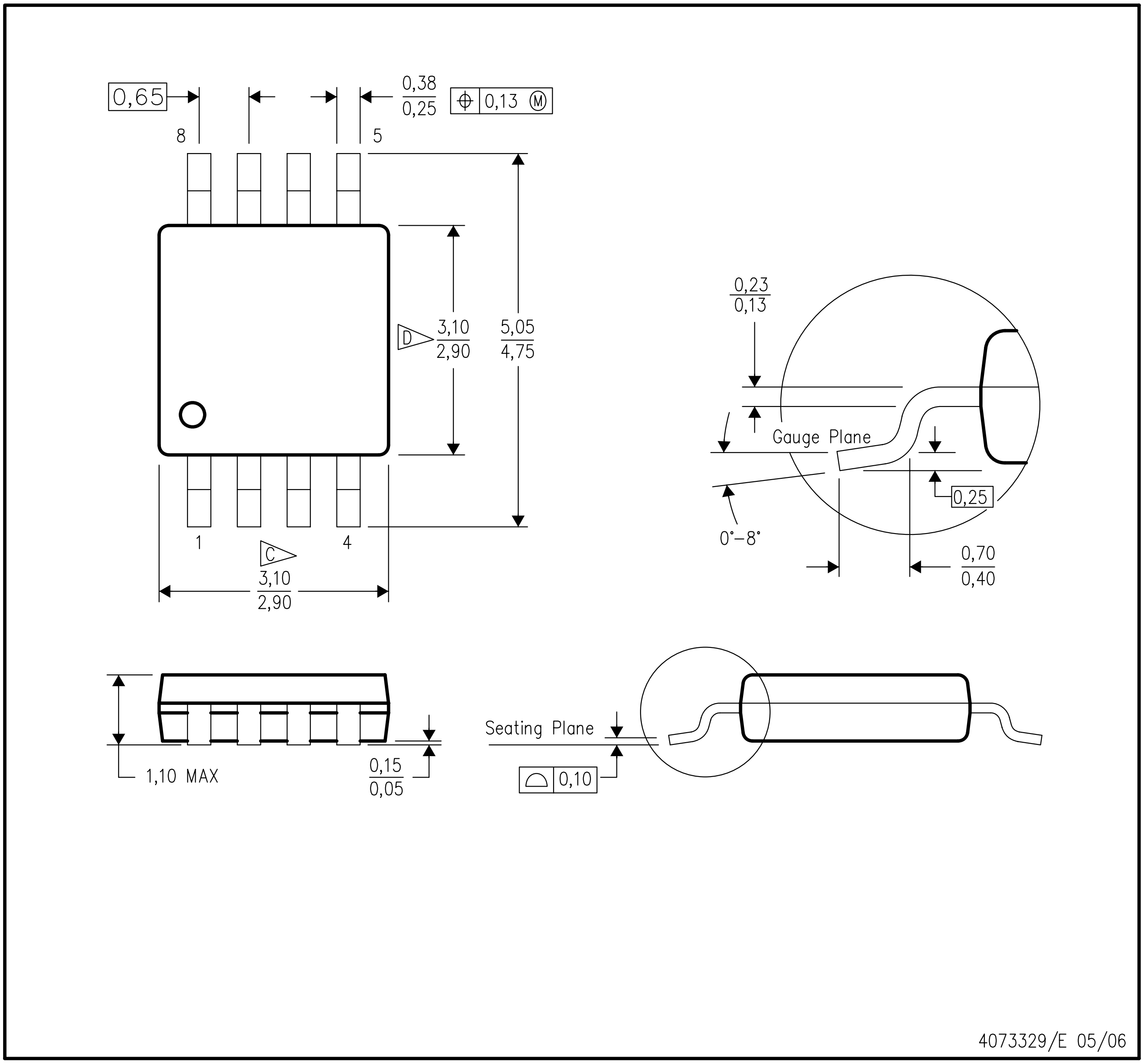
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
INA159AIDGKR	MSOP	DGK	8	2500	346.0	346.0	29.0
INA159AIDGKT	MSOP	DGK	8	250	184.0	184.0	50.0

DGK (S-PDSO-G8) PLASTIC SMALL-OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO-187 variation AA, except interlead flash.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265